Digital Design with Programmable Logic

16-bit Pseudorandom Number Generator

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Brief Summary

A description of what you did in the lab and what steps were followed

Lab 2 consisted of creating a clock divider (clock_divider.vg) module to slow down a 100MHz clock, creating a Galois LFSR-based PRNG module (lfsr.vg), and combining these to create a 16-bit pseudo-random number generator. Along with these modules, testbenches were created to test functionality before implementing onto the Boolean Board FPGA.

Then to implement the design on an FPGA, a top module was created, and the output drives a 7-segment display which displays the hex characters corresponding to the 16-bit pseudo-random number.

Discussion of Results

1) What were the test cases you used and discuss why you chose the set of test cases, what changes did you do to test the basic LFSR (without 7-seg)?

- The test cases I used for the basic LFSR was using a seed of 1 and seeing the shifted output of the PRNG where the taps were placed. This allows for the verification of an expected value

2) If you had to modify your design to meet your design, discuss what methodology you followed, etc. (i.e. to add the 7-seg display)

N/A

Reports

Simulation waveforms (behavioral) showing all the test cases used above. (w/o 7-seg)

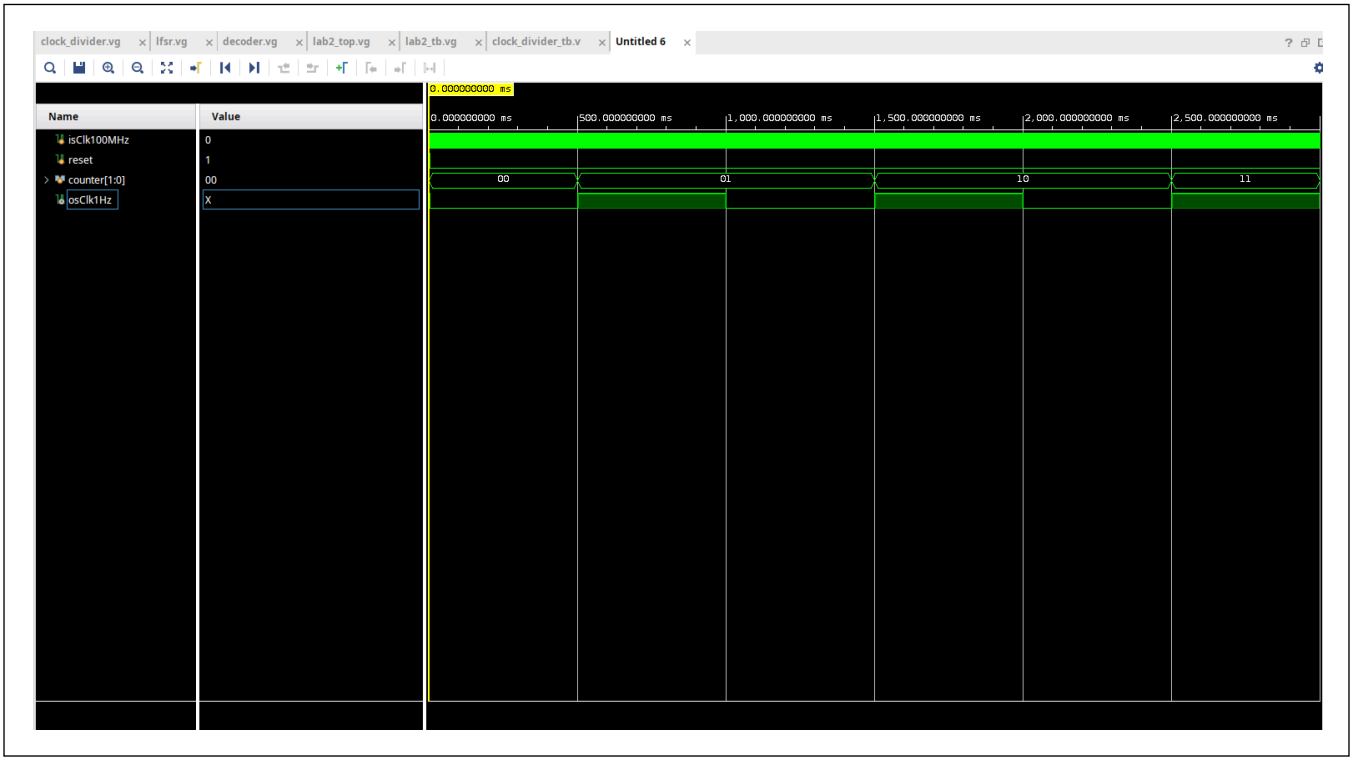

Figure 1: Clock divider Testbench showing a divider of a 100MHz clock to a 1MHz clock.

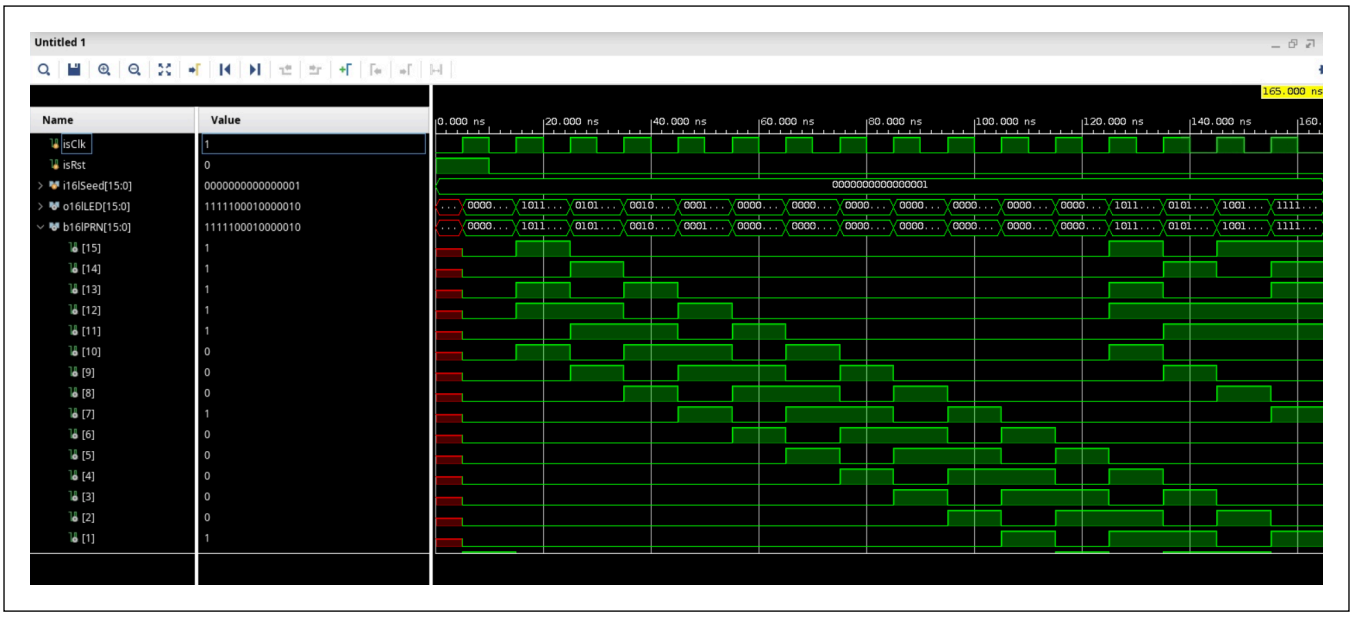

Figure 2: LFSR Testbench with seed of 1

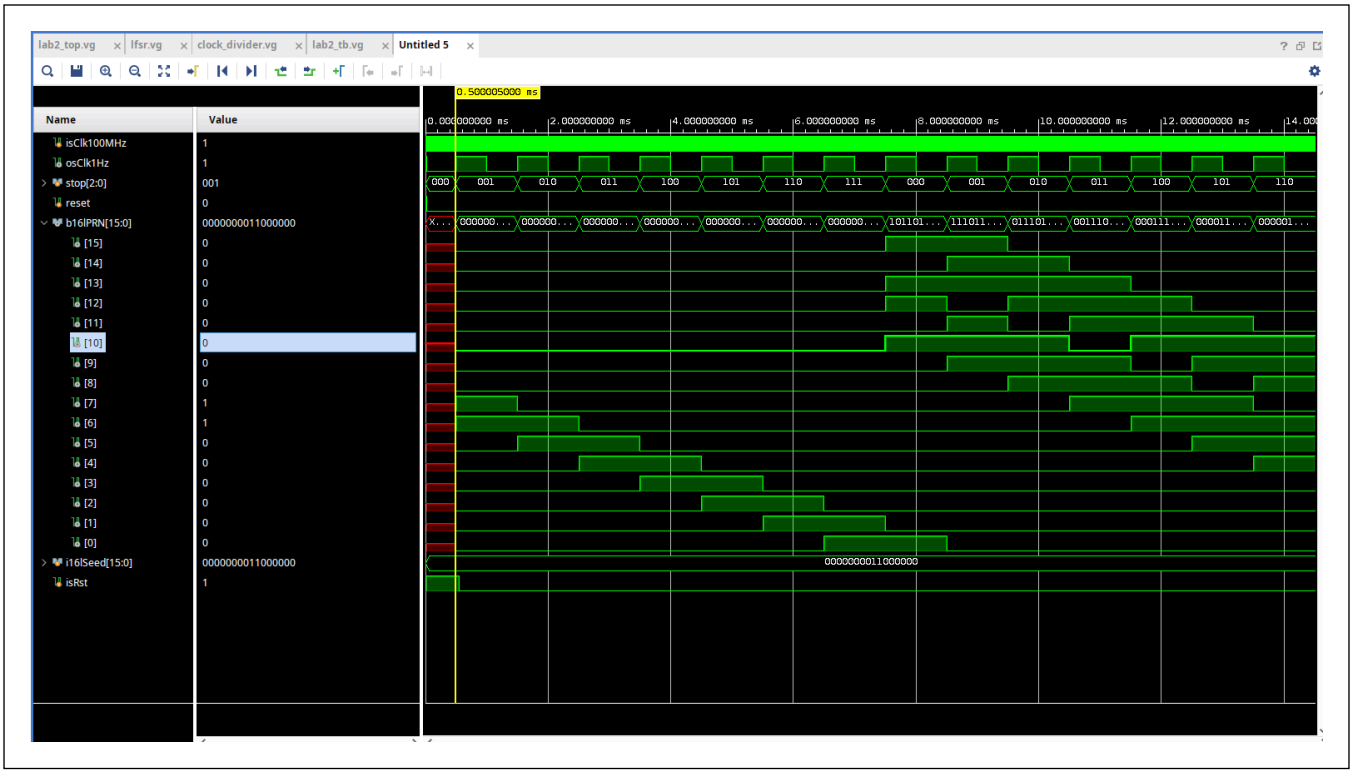

Figure 3: PRNG Testbench For a initial PRNG seed of 0000_0000_1100_0000

Elaboarated Design Schematic

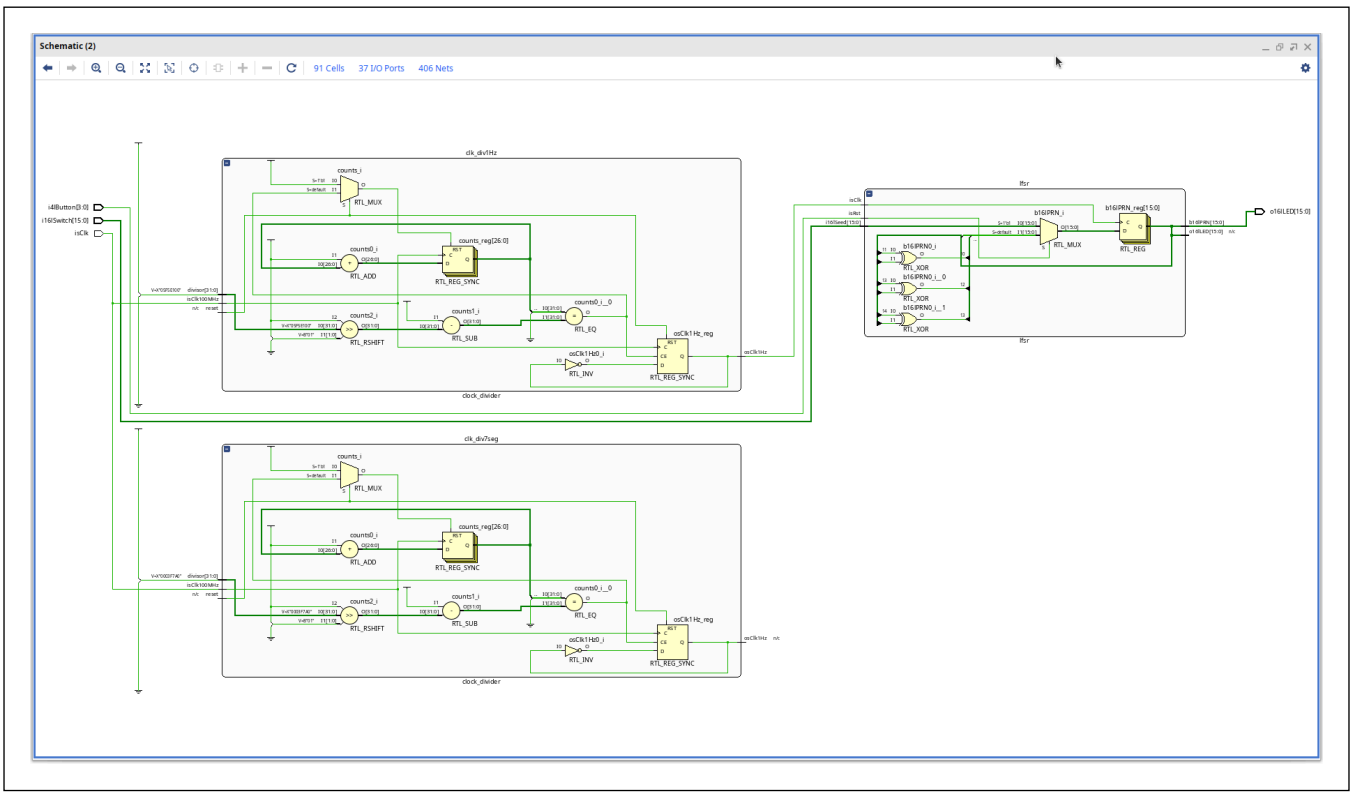

Figure 4: Elaborated Design Schematic

Synthesized Schematics

Figure 5: LFSR Synthesized design (w/o 7 seg)

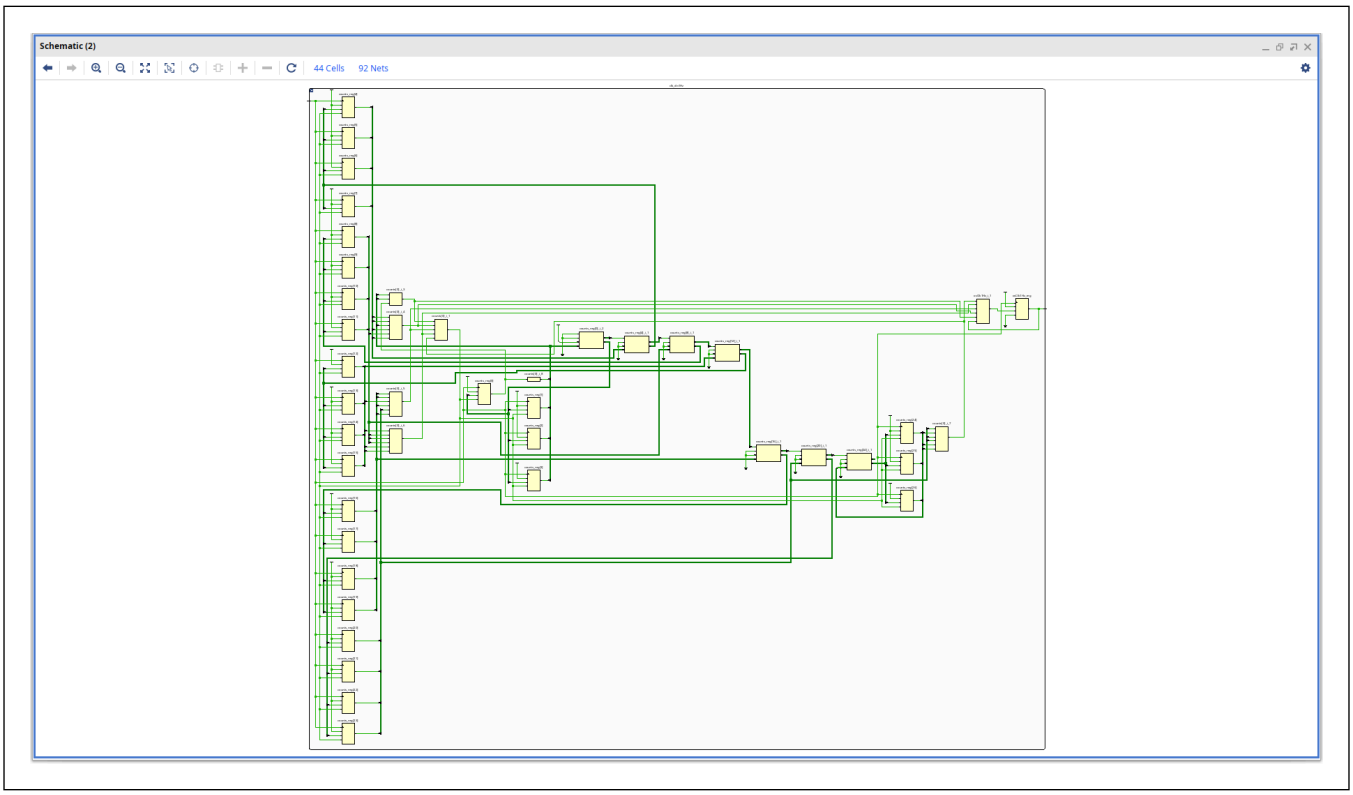

Figure 6: Clock Divider Synthesized design (w/o 7 seg)

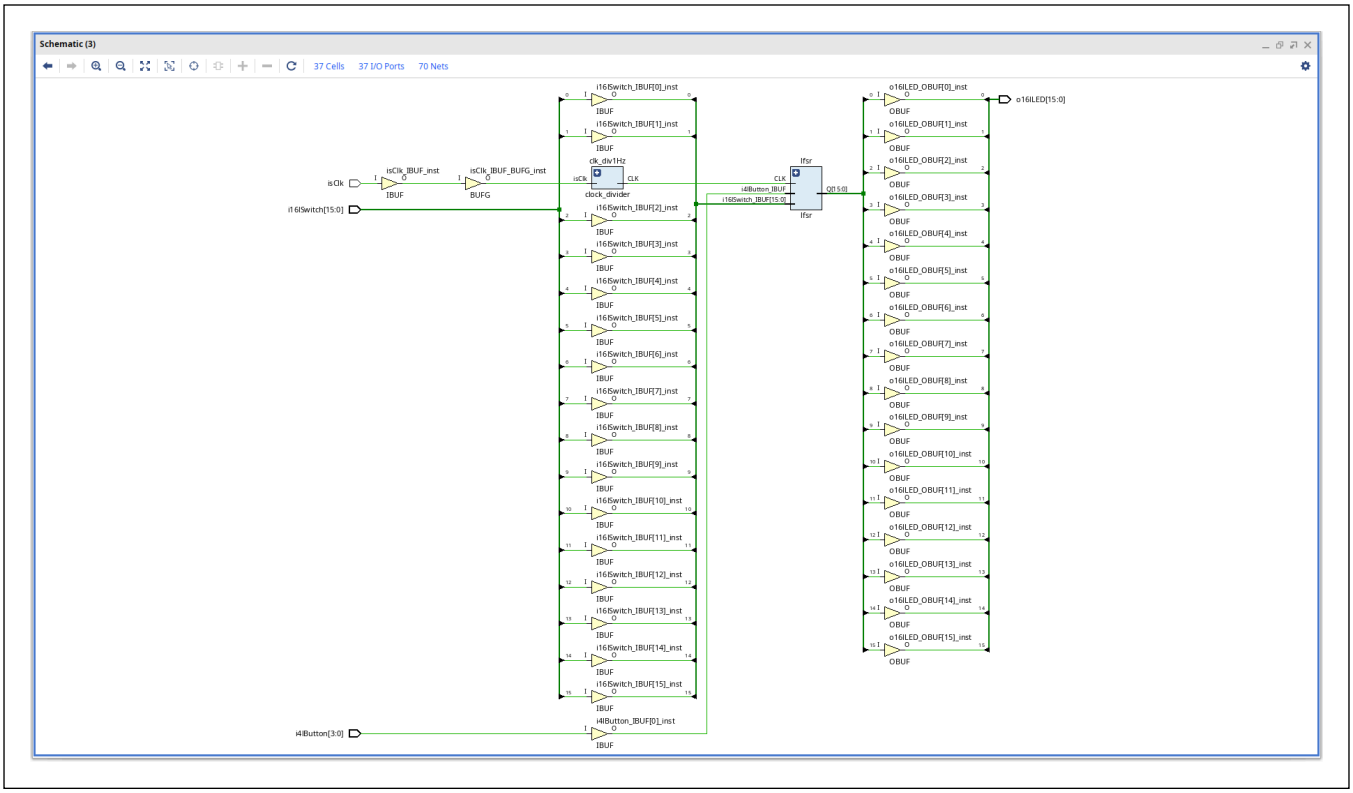

Figure 7: Top module schematic (w/o 7 seg)

Timing report (w/o 7-seg)

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             5.924ns  (required time - arrival time)
  Source:                 clk_div1Hz/counts_reg[15]/C
                            (rising edge-triggered cell FDRE clocked by isClk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            clk_div1Hz/counts_reg[20]/R
                            (rising edge-triggered cell FDRE clocked by isClk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             isClk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (isClk rise@10.000ns - isClk rise@0.000ns)
  Data Path Delay:        3.476ns  (logic 0.704ns (20.251%)  route 2.772ns (79.749%))
  Logic Levels:           2  (LUT5=1 LUT6=1)
  Clock Path Skew:        -0.136ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.779ns = ( 14.779 - 10.000 )
    Source Clock Delay      (SCD):    5.093ns
    Clock Pessimism Removal (CPR):    0.179ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock isClk rise edge)      0.000     0.000 r
    F14                                               0.000     0.000 r  isClk (IN)
                         net (fo=0)                   0.000     0.000    isClk
    F14                  IBUF (Prop_ibuf_I_O)         1.458     1.458 r  isClk_IBUF_inst/O
                         net (fo=1, routed)           1.972     3.430    isClk_IBUF
    BUFGCTRL_X0Y16       BUFG (Prop_bufg_I_O)         0.096     3.526 r  isClk_IBUF_BUFG_inst/O
                         net (fo=28, routed)          1.567     5.093    clk_div1Hz/isClk
    SLICE_X35Y48         FDRE                                       r  clk_div1Hz/counts_reg[15]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X35Y48         FDRE (Prop_fdre_C_Q)         0.456     5.549 r  clk_div1Hz/counts_reg[15]/Q
                         net (fo=2, routed)           0.833     6.383    clk_div1Hz/counts_reg[15]
    SLICE_X34Y49         LUT6 (Prop_lut6_I2_O)        0.124     6.507 r  clk_div1Hz/counts[0]_i_5/O
                         net (fo=2, routed)           0.965     7.471    clk_div1Hz/counts[0]_i_5_n_0
    SLICE_X34Y46         LUT5 (Prop_lut5_I2_O)        0.124     7.595 r  clk_div1Hz/counts[0]_i_1/O
                         net (fo=27, routed)          0.974     8.570    clk_div1Hz/p_0_in
    SLICE_X35Y50         FDRE                                       r  clk_div1Hz/counts_reg[20]/R
  -------------------------------------------------------------------    -------------------

                         (clock isClk rise edge)     10.000    10.000 r
    F14                                              0.000    10.000 r  isClk (IN)
                         net (fo=0)                  0.000    10.000    isClk
    F14                  IBUF (Prop_ibuf_I_O)        1.388    11.388 r  isClk_IBUF_inst/O
                         net (fo=1, routed)          1.868    13.256    isClk_IBUF
    BUFGCTRL_X0Y16       BUFG (Prop_bufg_I_O)        0.091    13.347 r  isClk_IBUF_BUFG_inst/O
                         net (fo=28, routed)         1.432    14.779    clk_div1Hz/isClk
    SLICE_X35Y50         FDRE                                       r  clk_div1Hz/counts_reg[20]/C
                         clock pessimism             0.179    14.958
                         clock uncertainty          -0.035    14.922
    SLICE_X35Y50         FDRE (Setup_fdre_C_R)      -0.429    14.493    clk_div1Hz/counts_reg[20]
  -------------------------------------------------------------------
                         required time                        14.493
                         arrival time                         -8.570
  -------------------------------------------------------------------
                         slack                                 5.924
```

Figure 8: Max Delay path with Slack (MET)

Power report (w/o 7-seg)

```
1.1 On-Chip Components
----------------------

+----------------+-----------+----------+-----------+-----------------+
| On-Chip        | Power (W) | Used     | Available | Utilization (%) |
+----------------+-----------+----------+-----------+-----------------+
| Clocks         |    <0.001 |        3 |       --- |             --- |
| Slice Logic    |    <0.001 |       96 |       --- |             --- |
|   LUT as Logic |    <0.001 |       17 |     32600 |            0.05 |
|   Register     |    <0.001 |       60 |     65200 |            0.09 |
|   CARRY4       |    <0.001 |        7 |      8150 |            0.09 |
|   BUFG         |    <0.001 |        1 |        32 |            3.13 |
|   Others       |     0.000 |        4 |       --- |             --- |
| Signals        |    <0.001 |      106 |       --- |             --- |
| I/O            |     0.021 |       34 |       210 |           16.19 |
| Static Power   |     0.072 |          |           |                 |
| Total          |     0.094 |          |           |                 |
+----------------+-----------+----------+-----------+-----------------+
```

Figure 9: Power Utilization Report (w/o 7-seg)

Utilization report: implementation (w/ 7-seg and w/o 7-seg)

```
227 | Report Cell Usage:
228 | +------+-------+------+
229 | |      |Cell   |Count |
230 | +------+-------+------+
231 | |1     |BUFG   |     1|
232 | |2     |CARRY4 |     7|
233 | |3     |LUT1   |     1|
234 | |4     |LUT3   |    14|
235 | |5     |LUT4   |     3|
236 | |6     |LUT5   |     1|
237 | |7     |LUT6   |     5|
238 | |8     |FDRE   |    44|
239 | |9     |IBUF   |    18|
240 | |10    |OBUF   |    16|
241 | +------+-------+------+
```

Figure 10: Synthesis Utilization Report Cell Usage (w/o 7 seg)

Summary or Conclusion:

1. Were all design goals met?
   - Yes all the design goals were met, I implemented the 16 bit LFSR based on the example given in Github with taps placed between the right bit locations. Additionally, the design was implemented onto an FPGA, and multiplexing logic was created for the 7-segment displays.
2. What were the difficulties encountered?
   - Doing the multiplexing for the 7 segment display, and the clock_divider.vg module was difficult. Specifically getting the dividing formula and calculations correct.
3. Any improvement you would like to make time permitting? Etc…
   - Not really, I think that learning how to code more efficient would be helpful, however I did make changes to the clock_divider module in the next lab to allow for the input of a value for a desired clock rate.