Lab 1 Hamming Code

[redacted] Digital Design With Programmable Logic Laboratory

[redacted] [redacted]

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I Hamming Simulation Waveforms)

Figure 1 below provides a reference to reading the simulation waveforms for the detected and undetected error cases.

```
$display("original      = %b", i16lSwitch[7:0]);
$display("inverted    = %b", i16lSwitch[15:8]);
$display("corrupted     = %b", o16lLED[7:0]);
$display("original parity    = %b", o16lLED[11:8]);
$display("inverted parity    = %b", o16lLED[15:12]);

if (o16lLED[11:8] == o16lLED[15:12]) begin
  $display("Parity matches - ERROR NOT DETECTED (4-bit corruption passed)");
end else begin
  $display("Parity mismatch - Error detected");
```

Figure 1: Reference to for signals in detected error case and undetected case waveforms.

I.i Working Case

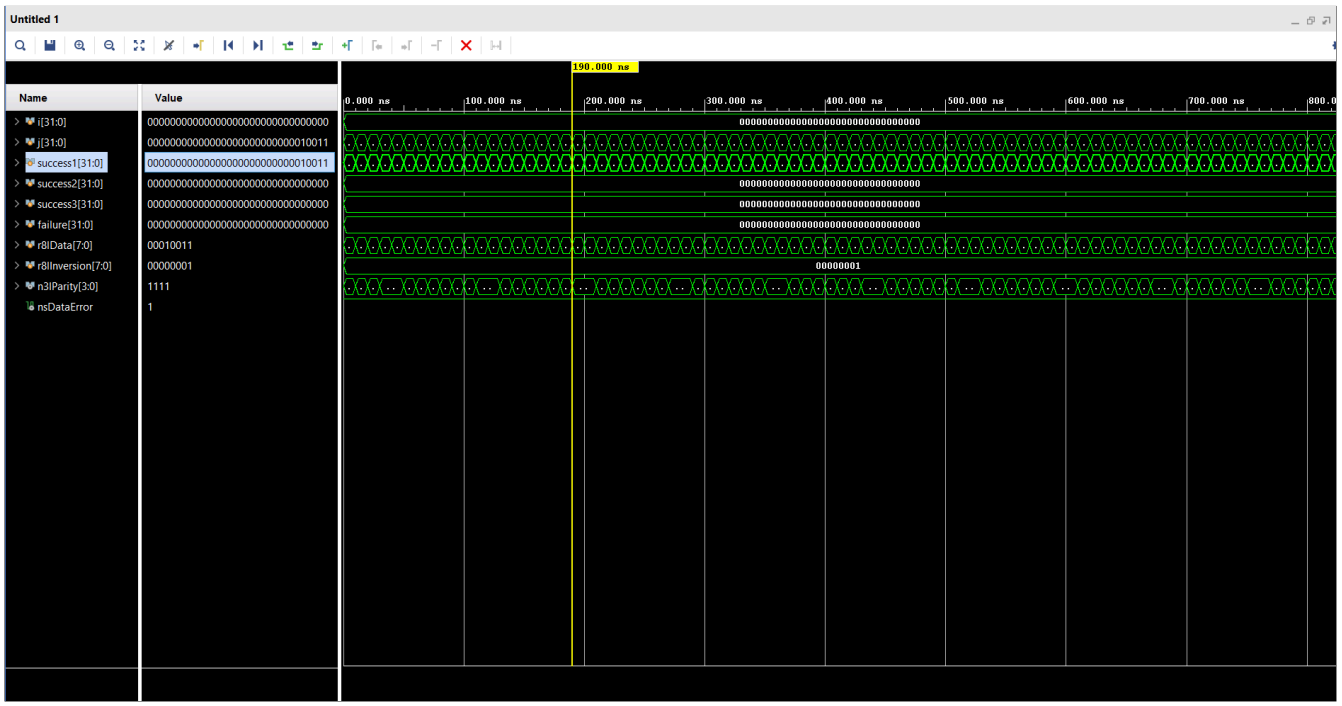

Figure 2: Hamming calculator working case

I.ii Detected Error Case

In the detected error case, with an inversion pattern of 1000_0011_0000_0001. Figure 4 displays the output of the test-bench for verification of the error detection.

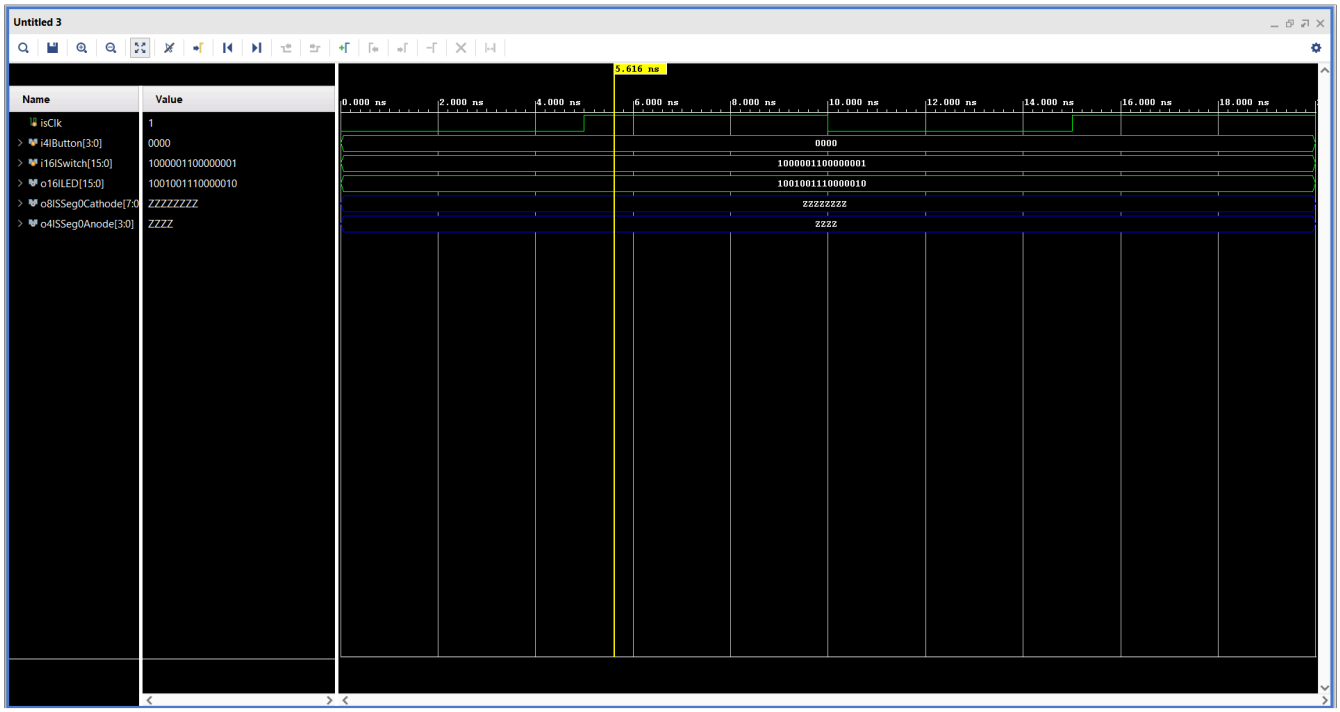

Figure 3: lab1_top Simulation waveform for a detected error case

```
original       = 00000001
inverted    = 10000011
corrupted      = 10000010
original parity     = 0011
inverted parity    = 1001
Parity mismatch - Error detected
```

Figure 4: lab1_top Simulation waveform for a detected error case

I.iii Undetected Error Case

In the detected error case, with an inversion pattern of 1010_0011_0000_0001. Figure 6 displays the output of the test-bench for verification of the error detection.

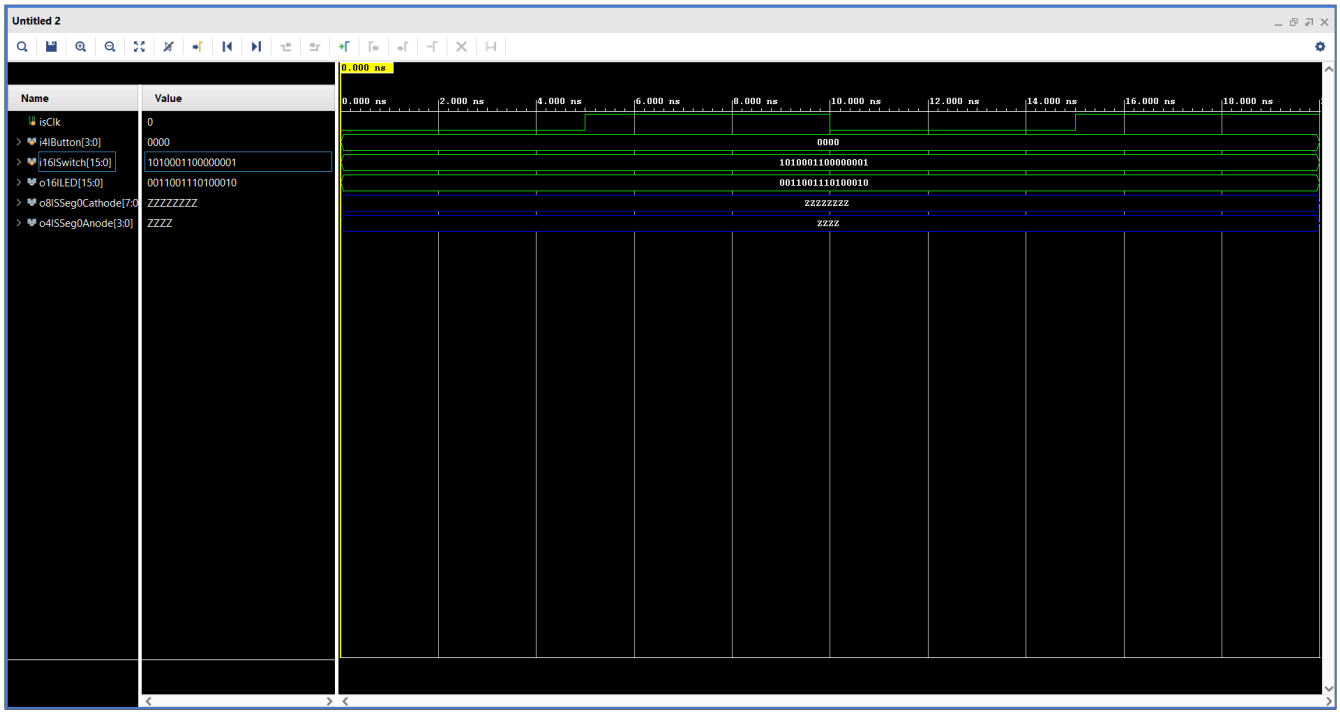

Figure 5: lab1_top Simulation waveform for an undetected error case

```
original       = 00000001
inverted    = 10100011
corrupted      = 10100010
original parity     = 0011
inverted parity    = 0011
Parity matches - ERROR NOT DETECTED (4-bit corruption passed)
```

Figure 6: lab1_top Simulation waveform for a detected error case

II Schematic (From RTL Analysis)

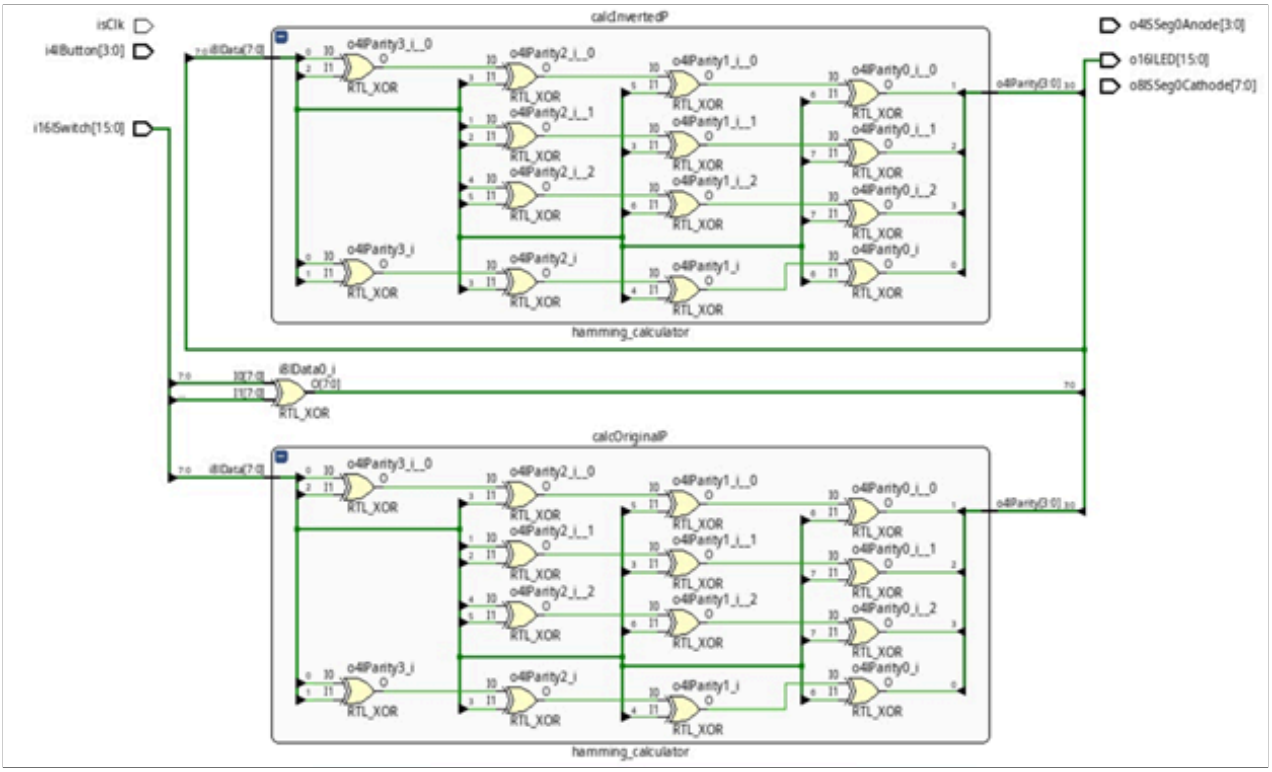

Figure 7: Schematic from RTL Analysis

III Post-Implementation Utilization Report

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs	13	0	32600	0.04
LUT as Logic	13	0	32600	0.04
LUT as Memory	0	0	9600	0.00
Slice Registers	0	0	65200	0.00
Register as Flip Flop	0	0	65200	0.00
Register as Latch	0	0	65200	0.00
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

Figure 8: Slice Logic from Post-Implementation Utilization Report

IV Power Report Summary

1.1 On-Chip Components

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	3	---	---
Slice Logic	<0.001	20	---	---
LUT as Logic	<0.001	13	32600	0.04
Others	0.000	2	---	---
Signals	<0.001	34	---	---
I/O	0.029	44	210	20.95
Static Power	0.072			
Total	0.102			

Figure 9: On chip components from Power Report Summary